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[Name of Document] SPECIFICATION

[Title of the Invention] CIRCUIT SUBSTRATE, MANUFACTURING METHOD THEREOF, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC APPARATUS

[Claims]

[Claim 1] A circuit substrate comprising:

a plurality of terminals formed on a substrate; and

one or more resistances formed between said terminals adjacent one to another;

wherein said plurality of terminals include analog terminals connected to analog signal lines for supplying analog signals, and digital terminals connected to digital signal lines for supplying digital signals;

and wherein said resistance which has at least one end thereof connected to said analog terminal, has a resistance value greater than said resistance connected between said digital terminals.

[Claim 2] A circuit substrate comprising:

a plurality of terminals formed on a substrate; and

one or more resistances formed between said terminals adjacent one to another;

wherein said plurality of terminals include first terminals connected to data lines for supplying data signals, and second terminals connected to control lines for supplying control signals;

and wherein said resistance which has at least one end thereof connected to said first terminal, has a resistance value greater than said resistance connected between said second terminals adjacent one to another.

[Claim 3] A circuit substrate comprising:

a common electrode line formed on the perimeter of a substrate;

a plurality of terminals formed on said substrate; and

one or more resistances formed between said terminals and said common electrode line;

wherein said plurality of terminals include analog terminals connected to analog signal lines for supplying analog signals, and digital terminals connected to digital signal lines for supplying digital signals;

and wherein said resistance connected to said analog terminal has a resistance value greater than said resistance connected to said digital terminal.

[Claim 4] A circuit substrate comprising:

a common electrode line formed on the perimeter of a substrate;

a plurality of terminals formed of said substrate;

one or more first resistances formed between said terminals adjacent one to another; and

one or more second resistances formed between said terminals and said common electrode line.

[Claim 5] A circuit substrate according to Claim 4, wherein said terminal is connected to both said first resistance and said second resistance;

and wherein said first resistance has a resistance value greater than said second resistance.

[Claim 6] A circuit substrate according to Claim 5, wherein said plurality of terminals include analog terminals connected to analog signal lines for supplying analog signals, and digital terminal connected to digital signal lines for supplying digital signals;

and wherein both said first resistance and said second resistance which have at least one end thereof connected to said analog terminal, have resistance values greater than both said first resistance which is connected between said digital terminals, and said second resistance which is connected between said digital terminal and said common electrode line.

[Claim 7] A circuit substrate according to any of Claim 1 through 6, further comprising:

electric power terminals connected to a power source; and

resistances formed between said electric power terminals and adjacent non-electric power terminals formed for purposes other than supplying power.

[Claim 8] A circuit substrate according to Claim 7,

wherein said resistance has a resistance value equal to or less than the resistance connected to other non-electric power terminals.

[Claim 9] A circuit substrate comprising:

a common electrode line formed on the perimeter of a substrate;

data line terminals connected to data lines for supplying analog signals;

control signal terminals connected to control signal lines for supplying digital signals;

electric power terminals for supplying negative electric power or positive electric power;

first resistances connected between said terminals adjacent one to another; and

second resistances connected between said terminals.

[Claim 10] A circuit substrate according to Claim 9, wherein, in the event that any of said terminals are connected to both said first resistance and said second resistance, said first resistance has a resistance value greater than said second resistance.

[Claim 11] A circuit substrate according to Claim 10, wherein both said first resistance and said second resistance which have at least one end thereof connected to said data terminal, have resistance values greater than any of said first resistance connected between said control

signal terminals, said first resistance connected between said control signal terminal and said electric power terminal, said second resistance connected between said control signal terminal and said common electrode line, and said second resistance connected between said electric power terminal and said common electrode line.

[Claim 12] A circuit substrate according to any of Claim 1 through Claim 11, wherein said resistances are formed of a semiconductor film.

[Claim 13] A circuit substrate according to any of Claim 1 through Claim 11, wherein said resistance includes a protection circuit configuration employing PN junction configurations with reverse polarity.

[Claim 14] An electro-optical device including a circuit substrate according to any of Claim 1 through Claim 13.

[Claim 15] An electronic apparatus including an electro-optical device according to Claim 14.

[Claim 16] A manufacturing method for a circuit substrate including a common electrode line on the perimeter thereof and a plurality of terminals on the inner side of said substrate from said common electrode line, comprising:

a step for forming one or more first resistance configurations on regions between said terminals adjacent one to another;

a step for forming one or more second resistance

configurations on regions between said terminals and said common electrode line;

a step for forming said terminals which are electrically connected to a part of said first resistance configurations or/and said second resistance configurations; and

a step for forming said common electrode lines which are electrically connected to a part of said second resistance configurations.

[Claim 17] A manufacturing method for a circuit substrate according to Claim 16, wherein said first resistance configurations and said second resistance configurations are formed so that said first resistance configuration has a resistance value greater than said second resistance configuration.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a circuit substrate used for an electro-optical device such as a display panel or the like, and particularly to a configuration for improving prevention of electrostatic breakdown during manufacturing or operating of the circuit substrate.

[0002]

[Description of the Related Art]

With some circuit substrates used for electro-optical devices such as active-matrix-driven liquid crystal display panels, EL (electro-luminescence) display panels, or the like, arrangements have been known wherein an electrostatic-protection configuration is provided for preventing breakdown of the internal circuit due to static electricity occurring during manufacturing or operation.

[0003]

As conventional electrostatic-protection configurations, arrangements are known wherein terminals are connected with protection patterns with the adjacent terminals short-circuited or connected with a resistance during manufacturing, and the protection patterns are cut off following completion as disclosed in Japanese Unexamined Patent Application Publication No. 58-116573 (Patent document 1) or Japanese Unexamined Patent Application Publication No. 63-106788 (Patent document 2), or arrangements are known wherein all the disposed terminals are short-circuited along the perimeter of the substrate outward from the disposed terminals during manufacturing as disclosed in Japanese Unexamined Patent Application Publication No. 2-24229 (Patent document 3), Japanese Unexamined Patent Application Publication No. 7-181516 (Patent document 4), and Japanese Unexamined Patent Application Publication No. 7-175086 (Patent document 5).

[0004]

Furthermore, electrostatic protection configurations have been presented wherein resistances in the range causing no problem with regard to operation of the data lines and the scan lines are added, and accordingly, a step for cutting off the protection patterns can be eliminated even following electrical testing, and also electrostatic breakdown can be prevented in the final product, as disclosed in Japanese Unexamined Patent Application Publication No. 63-085586 (Patent document 6), Japanese Unexamined Patent Application Publication No. 2-061618 (Patent document 7), Japanese Unexamined Patent Application Publication No. 6-273783 (Patent document 8), and Japanese Unexamined Patent Application Publication No. 8-179360 (Patent document 9).

[0005]

[Patent document 1] Japanese Unexamined Patent Application Publication No. 58-116573

[Patent document 2] Japanese Unexamined Patent Application Publication No. 63-106788

[Patent document 3] Japanese Unexamined Patent Application Publication No. 2-24229

[Patent document 4] Japanese Unexamined Patent Application Publication No. 7-181516

[Patent document 5] Japanese Unexamined Patent Application

Publication No. 7-175086

[Patent document 6] Japanese Unexamined Patent Application Publication No. 63-085586

[Patent document 7] Japanese Unexamined Patent Application Publication No. 2-061618

[Patent document 8] Japanese Unexamined Patent Application Publication No. 6-273783

[Patent document 9] Japanese Unexamined Patent Application Publication No. 8-179360

[0006]

[Problems to be Solved by the Invention]

However, no particular arrangements have been disclosed wherein a circuit substrate including a layout for supplying various types of signals such as analog signals and digital signals and various kinds of potential has a configuration for efficiently preventing electrostatic breakdown while preventing cross-talk.

[0007]

Furthermore, while configurations having predetermined protection patterns at each terminal have been disclosed, the relation between the protection patterns ~~have~~ has not been disclosed.

[0008]

The present invention has been made to solve the above-described problems, and it is an object thereof to provide a

circuit substrate, manufacturing method thereof, electro-optical device, and electronic apparatus, having electrostatic-breakdown-prevention functions suitable for a layout for supplying various types of signals such as analog signals and digital signals and various kinds of potential.

[0009]

[Means for Solving the Problems]

A circuit substrate according to the present invention comprises multiple terminals formed on a substrate, and one or more resistances formed between the terminals adjacent one to another. The multiple terminals include analog terminals connected to analog signal lines for supplying analog signals, and digital terminals connected to digital signal lines for supplying digital signals. Furthermore, the resistance which has at least one end thereof connected to said analog terminal, has a resistance value greater than the resistance connected between the digital terminals.

[0010]

Analog signals are influenced by cross-talk, and accordingly, there is the need to reduce the influence of the adjacent lines as compared with digital signals while maintaining prevention of electrostatic breakdown. With the present invention, the resistance connected to an analog terminal is greater than the resistance connected to a digital terminal, thereby providing the advantage of

suppressing cross-talk to a minimum in the analog terminals while maintaining protection of all the terminals from static electricity with the resistances.

[0011]

Note that "connecting to an analog terminal" means that at least one end of a resistance is connected to an analog terminal, and "connecting between digital terminals" means that both ends of a resistance are connected between digital terminals.

[0012]

Furthermore, with the present invention, "circuit substrate" means a substrate wherein wiring has been made for supplying various kinds of signals and potential, and the circuit configuration thereof is not restricted to a particular one. For example, the circuit substrate may be a display panel substrate having a display function, or may be a substrate used for a computer.

[0013]

Furthermore, with the present invention, "resistance" means not only a resistance-film configuration, having a predetermined resistance value, formed of a semiconductor film such as polysilicon or the like, but also a protection circuit employing the forward voltage characteristic and reverse voltage drop due to the PN junction of a semiconductor, which is employed along with or instead of

the resistance-film configuration. For example, the resistance may include a protection circuit configuration employing PN junction configurations in the reverse directions (e.g., configuration wherein diodes in the forward direction and the reverse direction are connected in parallel).

[0014]

Furthermore, a circuit substrate according to the present invention comprises a common electrode line formed on the perimeter of a substrate, multiple terminals formed on the substrate, and one or more resistances formed between the terminals and the common electrode line, wherein the multiple terminals include analog terminals connected to analog signal lines for supplying analog signals, and digital terminals connected to digital signal lines for supplying digital signals. Furthermore, the resistance connected to the analog terminal has a resistance value greater than the resistance connected to the digital terminal.

[0015]

Furthermore, a circuit substrate according to the present invention comprises a common electrode line formed on the perimeter of a substrate, multiple terminals formed on the substrate, one or more first resistances formed between the terminals adjacent one to another, and one or

more second resistances formed between the terminals and the common electrode line.

[0016]

That is to say, with a configuration wherein the first resistance and the second resistance are connected in parallel, even in the event that the first resistance between an analog terminal and the adjacent terminal has a somewhat great resistance value, the total resistance value is greatly reduced due to the parallel connection, thereby efficiently providing prevention of electrostatic breakdown.

[0017]

In this case, with a configuration wherein a terminal is connected to both the first resistance and the second resistance, the first resistance preferably has a resistance value greater than the second resistance. The second resistance connected to the common electrode line has a low resistance value, and accordingly, greater electrostatic current flows in the second resistance, thereby efficiently preventing the internal circuit from electrostatic discharge.

[0018]

In this case, the multiple terminals include analog terminals connected to analog signal lines for supplying analog signals, and digital terminal connected to digital signal lines for supplying digital signals. Furthermore, both the first resistance and the second resistance which

have at least one end thereof connected to the analog terminal, have resistance values greater than both the first resistance which is connected between the digital terminals, and the second resistance which is connected between the digital terminal and the common electrode line. The analog terminal for transmitting analog signals, where cross-talk tends to occur, is connected to a resistance greater than with the digital terminal, thereby suppressing cross-talk to a minimum while maintaining prevention of electrostatic breakdown.

[0019]

A modification of the above-described circuit substrate according to the present invention further comprises electric power terminals connected to a power source, and resistances formed between the electric power terminals and adjacent non-electric power terminals formed for purposes other than supplying power. The electric power terminals are formed with low impedance, and accordingly, with the modification, the non-electric power terminals are connected to the electric power terminals with resistances, thereby efficiently preventing electrostatic breakdown.

[0020]

In this case, the resistance has a resistance value equal to or less than the resistance connected to other non-electric power terminals. With the modification, the

electric power terminal is connected to a resistance having relatively low resistance value in the same way as with the common electrode line, and accordingly, greater electric current flows to the electric power terminal through the resistance.

[0021]

A circuit substrate according to the present invention comprises a common electrode line formed on the perimeter of a substrate, data terminals connected to data lines for supplying analog signals, control signal terminals connected to control signal lines for supplying digital signals, electric power terminals for supplying negative electric power or positive electric power, first resistances connected between the terminals adjacent one to another, and second resistances connected between the terminals.

[0022]

In this case, in the event that any of said terminals are connected to both the first resistance and the second resistance, the first resistance preferably has a resistance value greater than the second resistance. The second resistance connected to the common electrode line has a low resistance, and accordingly, greater electrostatic current flows to the second resistance, thereby efficiently protecting the internal circuit from electrostatic discharge.

[0023]

In this case, both the first resistance and the second resistance which have at least one end thereof connected to the data terminal, preferably have resistance values greater than any of the first resistance connected between the control signal terminals, the first resistance connected between the control signal terminal and the electric power terminal, the second resistance connected between the control signal terminal and the common electrode line, and the second resistance connected between the electric power terminal and the common electrode line. The data terminals transmit analog signals wherein cross-talk tends to easily occur, and accordingly, with the circuit substrate, the resistance connected to the data terminal preferably has a great resistance value in order to suppress cross-talk to a minimum while maintaining prevention of electrostatic breakdown.

[0024]

An electro-optical device according to the present invention includes a circuit substrate having a configuration according to the present invention, and furthermore, an electronic apparatus according to the present invention includes the aforementioned electro-optical device.

[0025]

Here, "electro-optical device" means a device for

converting the change in electric signals into the change in light using electro-optical effects, and while not restricted to any particular one, typical examples include a liquid crystal display panel having a configuration so as to drive a liquid crystal layer with the active-matrix driving method, an EL display panel having a configuration so as to drive EL devices, and the like.

[0026]

Furthermore, "electronic apparatus" means an apparatus which includes an electro-optical device as a component so as to have predetermined functions, and while not restricted to any particular one, typical examples include cellular phones, video cameras, personal computers, head mount displays, rear or front projectors, facsimile apparatuses with display functions, digital camera viewfinders, portable TV sets, DSP devices, PDAs, palmtops, and the like.

[0027]

Furthermore, a manufacturing method according to the present invention, for a circuit substrate including a common electrode line on the perimeter thereof and multiple terminals on the inner side of the substrate from the common electrode line, comprises a step for forming one or more first resistance configurations on regions between the terminals adjacent one to another, a step for forming one or more second resistance configurations on regions between the

terminals and the common electrode line, a step for forming the terminals which are electrically connected to a part of the first resistance configurations or/and the second resistance configurations, and a step for forming the common electrode line which is electrically connected to a part of the second resistance configurations.

[0028]

Note that there is no need to separate the step for forming the first resistance configuration and the step for forming the second resistance configuration. Both the resistance configurations may be formed in a single step using a single resistance film. In the same way, there is no need to separate the step for forming the terminals and the step for forming the common electrode line. Both the terminals and the common electrode line may be formed in a single step using a single metal layer.

[0029]

In this case, the first resistance configurations and the second resistance configurations are preferably formed so that the first resistance configuration has a resistance value greater than the second resistance configuration. The second resistance connected to the common electrode line has a low resistance value, and accordingly, greater electrostatic current flows to the second resistance, thereby efficiently protecting the internal circuit from

electrostatic discharge.

[0030]

[Description of the Embodiments]

Description will be made now regarding embodiments according to the present invention with reference to the drawings.

<First Embodiment>

With a first embodiment of the present invention, the present invention is applied to a circuit substrate for forming an EL display panel including EL devices as electro-optical devices. In particular, the present embodiment relates to a circuit substrate with a control signal line for transmitting digital signals for a scan circuit and a data line for transmitting analog signals adjacent one to another.

[0031]

Fig. 1 is a plan view of an EL display panel 1 according to the present first embodiment. As shown in Fig. 1, the circuit substrate 1 comprises cathode lines 10a and 10b, anode lines 11a and 11b, scan circuits 12a and 12b, a data line group 13, and a scan line group 14, disposed on a substrate 100. With the present embodiment, a large display panel is employed, and accordingly, each pair of the identical circuits are disposed with the image display area DA introduced therebetween, and electric power, signals, and

the like, are supplied from both sides thereof.

[0032]

The cathode lines 10a and 10b serve as contact regions to the cathode which is a common electrode. An unshown cathode electrode film is formed so as to be connected to the aforementioned cathode lines and so as to cover the entire substrate, thereby enabling electrostatic current to be supplied to a luminescence layer (not shown) of the EL devices formed between both electrodes formed at each unshown pixel. The anode lines 11a and 11b are formed for providing power lines between the scan lines for supplying electric power to each pixel with low impedance. The scan circuits 12a and 12b have a configuration for scanning a desired scan line 14 according to control signals.

[0033]

Multiple terminals are formed on the substrate 100 along the longitudinal sides, wherein each line is connected to each terminal. Cathode terminals Vc are connected in parallel to multiple terminals in order to reduce the impedance thereof. Anode terminals VG, VB, and VR, are formed so as to supply independent electric power for each of the three primary colors, and multiple terminals are disposed for each of the three primary colors in order to reduce the impedance thereof. The control signal terminals C1 through C6 are formed for supplying control signals for

the scan circuit 12a and 12b. The data supplied from the terminals includes digital signals for control and electric power for the scan circuits. The data line terminals XnR, XnG, and XnB, ($1 \leq n \leq N$) serve as terminals for connecting each of data lines 13. With the configuration shown in Fig. 1, data line terminals are disposed so that pixels adjacent in the longitudinal direction are connected to the terminal units made up of three terminals for red, green, and blue, on alternating longitudinal sides thereof in order to reduce non-uniformity in display due to voltage drop in the data lines. While pixel circuits disposed within the image display area DA are not shown for simplifying description, each pixel circuit is disposed so as to be connected to one of the data lines and one of the scan lines of the active matrix formed of the data line group 13 and the scan line group 14. With the above-described configuration, data is written to each pixel circuit through the data line so that the EL device within the pixel circuit emits light with output corresponding to the aforementioned written data by selection of the scan line and control from an unshown emission control line.

[0034]

On the other hand, a common electrode 101 is formed on the substrate 100 at the perimeter thereof so as to surround the substrate 100. Furthermore, a resistance region 102

according to the present invention is formed so as to contain each terminal and so as to be connected to the common electrode 101. The adjacent terminals are electrically connected one to another with a resistance (first resistance) between the adjacent terminals formed on the resistance region 102, and each terminal is electrically connected to the grounded potential with a resistance (second resistance) between the terminal and the common electrode, thereby enabling electrostatic breakdown to be prevented.

[0035]

Next, description will be made regarding the relation of connection between the terminals, the common electrode, and the resistances, on the resistance region 102, with reference to Fig. 2. In order to further simplify description, the great number of identical terminals are not shown in Fig. 2.

[0036]

As shown in Fig. 2, with the present first embodiment, the cathode terminals VC, the anode terminals VR, VG, and VB, the control signal terminals CX and CY, and the data line terminals X1 and X2, are disposed in that order from the outer perimeter to the inner side of the substrate. Of these terminals, the data line terminals serve as analog terminals for transmitting analog signals, and the control

signal terminals serves as digital terminals for transmitting digital signals. The cathode terminals are electrically connected to the common electrode, and the anode terminals serve as electric power terminals. Note that, in a case that the electric power of the anode is actively changed, an arrangement may be made wherein the anode terminals serve as digital terminals for a countermeasure against electrostatic breakdown.

[0037]

Resistances R1 are formed between: each of the cathode terminals VC, the anode terminals VR, VG, and VB, and the control signal terminals CX and CY; and the common electrode 101. Furthermore, resistances R3 are formed between adjacent terminals of the cathode terminals VC, the anode terminals VR, VG, and VB, and the control signal terminals CX and CY. Furthermore, resistances R4 are formed between the adjacent terminals of the data line terminals X1, X2, …, and between the data terminal X1 and the control signal terminal CY. Furthermore, resistances R2 are formed between: each of the data line terminals X1 and X2; and the common electrode 101.

[0038]

With the present invention, the resistance wherein at least one end is connected to an analog terminal has a resistance value greater than the resistance connected to

adjacent digital terminals. That is to say, of the resistances connected between adjacent terminals, the resistance R4 connected to the data line terminal X1 or the like is set to have a resistance value greater than the resistance R3 connected to the control signal terminals CX and CY (R3 < R4). Analog signals are influenced by cross-talk, and accordingly, the influence of the adjacent lines should be reduced as compared with digital signals even while maintaining prevention of electrostatic breakdown. With the present invention, the resistance connected to the analog terminal is greater than the resistance between the digital terminals, and accordingly, cross-talk can be reduced to a minimum in analog terminals while maintaining prevention of electrostatic breakdown in all the terminals.

[0039]

Furthermore, with the present invention, the resistance connected to the analog terminal is greater than the resistance connected to the digital terminal. That is to say, of the resistances connected between each terminal and the common electrode, the resistance R2 connected to the data line terminal X1 or the like is set to have a resistance value greater than the resistance R1 connected to the control signal terminals CX and CY (R1 < R2). The reason is the same as above.

[0040]

Furthermore, with the present invention, the resistance value of the first resistance formed between the adjacent terminals is greater than that of the second resistance formed between any of the aforementioned terminals and the common electrode. That is to say, with regard to the resistances R4 and R2 connected to the data line terminal, R4 serving as the first resistance ~~is set to a resistance~~is set to have a resistance value greater than R2 serving as the second resistance, and with regard to the resistances R3 and R1 connected to the signal control terminal, R3 serving as the first resistance ~~is set to a resistance~~is set to have a resistance value greater than R1 serving as the second resistance. With the above-described configuration, the second resistances R2 and R1 connected to the common electrode 101 are set to have small resistance values, and accordingly, electrostatic current is greater as compared with the first resistances R4 and R3, thereby efficiently preventing the internal circuit from electrostatic breakdown.

[0041]

Furthermore, with the present invention, both of the first and second resistances wherein at least one end thereof is connected to the analog terminal have resistance values greater than both of the first resistance connected between the adjacent digital terminals and the second resistance connected between the aforementioned digital

terminal and the common electrode.

That is to say, both of the resistances R2 and R4 connected to the data line terminals X1 or X2 are set have to resistance values greater than both of resistances R3 and R1 which are not connected to any data line terminal and are connected to the control signal terminals CX or CY. The analog terminals, wherein cross-talk tends to easily occur, have greater resistance values, and thus, cross-talk can be suppressed to a minimum while maintaining prevention of electrostatic breakdown.

[0042]

Furthermore, with the present invention, a resistance is formed between an electric power terminal and the adjacent non-electric-power terminal. That is to say, the anode terminal VB is adjacent to the control signal terminal CX, wherein the resistance R3 is formed therebetween. In general, the power electric terminals have low impedance, and accordingly, with the configuration of the present invention, electric power terminals are connected to the non-electric-power terminals with resistances, thereby efficiently preventing electrostatic breakdown.

[0043]

Note that the resistance connected to the electric power terminal has a resistance value equal to or less than the resistance connected to other non-electric-power

terminals. That is to say, the resistance connected to any of the anode electrodes VR, VG, and VB, are set to have a resistance value equal to or less than the resistance connected to any of the control signal terminals CX and CY. In general, power electric terminals have low impedance, and accordingly, with the configuration of the present invention, electric power terminals are connected to the non-electric-power terminals with relatively low resistances, so even greater electrostatic current can be transmitted to the electric power terminals through resistances connected to the electric power terminals.

[0044]

Summarizing the above-described relation, the relation $R1 << R3 < R2 < R4$ holds with regard to the resistance values on the resistance region 120. Note that electrostatic breakdown can be prevented even in the event that the above-described relation is not satisfied.

[0045]

Next, description will be made regarding a layer configuration of the resistance region 102 with reference to an enlarged plan view shown in Fig. 3(a) and cross-sectional diagram shown in Figs. 3(b) through 3(e). These drawings are enlarged diagrams for a region containing two terminals (T1 and T2) and the common electrode 101. Each resistance has a similar resistance configuration even while the

resistances have different resistance values, and accordingly, the configurations of these terminals can be understood in the same way.

[0046]

A resistance configuration between adjacent terminals (first resistance configuration) Rx serves as a resistance between the terminals T1 and T2, and is determined by the width Wx and the distance DX between adjacent terminals in the plan view. A resistance configuration Ry between a terminal and the common electrode (second resistance configuration) serves as a resistance between: any of the terminals T1 and T2; and the common electrode CE, and is determined by the width Wy and the distance Dy between adjacent terminals in the plan view. These resistance configurations Rx and Ry are formed of a semiconductor film. Taking the thickness of the semiconductor film to be constant, the resistance value of each resistance configuration is determined corresponding to the width W and the distance D. That is to say, with the resistivity of the semiconductor film as ρ, and with the thickness of the semiconductor film as t, the relation $R = \rho \cdot D/(W \cdot t)$ holds. Accordingly, each desired resistance value according to the above-described relation can be provided by adjusting the width and distance of the patterned semiconductor film. Note that it is needless to say that the resistance value

may be controlled by adjusting the thickness of the semiconductor film or adjusting concentration of impurities. That is to say, in the event of increasing the thickness of the semiconductor film, the cross-sectional area of the semiconductor film is increased, and accordingly, the resistance value is reduced corresponding thereto, and conversely, in the event of reducing the thickness, the cross-sectional area is reduced, and accordingly, the resistance value is increased. On the other hand, the greater the concentration of impurities is, the smaller the resistance value is, and conversely, the smaller the concentration of the impurities is, the greater the resistance is.

[0047].

Next, description will be made regarding layer configurations of the resistance configurations. As shown in Figs. 3(b) through 3(e), these resistance configurations are formed by patterning a semiconductor film 201 formed on a substrate 200 in the corresponding form. An insulating film 202 is formed on the semiconductor film 201, and a metal layer 203 is further formed thereon so as to be patterned in the forms of terminals, lines, and common electrodes. As described above, each resistance value can be controlled by adjusting the patterned form of the semiconductor film 201.

[0048]

Description will be made below in brief regarding a manufacturing method for the above-described resistance configurations.

First of all, the semiconductor film 201 is formed on the glass substrate 200 formed of silica glass, non-acrylic glass, or the like. While the semiconductor film is preferably formed of polysilicon due to the suitable resistance of polysilicon of several kΩ/square, an arrangement may be made wherein the semiconductor layer is formed of a high-resistivity material such as amorphous silicon, ITO, or the like. The semiconductor film is formed with the formation method wherein amorphous silicon is deposited with the low-temperature plasma CVD method, and subsequently, the deposited amorphous silicon film is crystallized by a laser such as an excimer laser or the like, for example. Note that an arrangement may be made wherein the semiconductor film is formed with other known method, e.g., the spin coating method, the droplet-discharge method, the low pressure chemical vapor deposition method (LPCVD method), or the CVD method. The thickness of the semiconductor film 201 is determined based upon the required resistance value and the form of the semiconductor film.

[0049]

Following formation of the semiconductor film,

patterning is performed with a known photolithography method or the like so as to form required resistance configurations. Note that, in the event of directly forming patterns with the droplet-discharge method, patterning processing on the substrate can be eliminated.

[0050]

Next, the insulating film 202 is formed. The insulating film 202 can be formed of silicon oxide, silicon nitride, or TEOS (tetra-ethoxy-silane), for example. While the insulating film 202 is preferably formed with the plasma CVD method, the insulating film may be formed with other known methods, e.g., a coating method such as the spin coating method or a droplet-discharge method such as the ink-jet method, wherein polysilazane dissolved in solvent is coated and heated, the low-pressure chemical vapor deposition method (LPCVD method), or the chemical vapor deposition method, wherein a silicon oxide film or silicon nitride film is formed.

[0051]

Last of all, the metal layer 203 is formed with the sputter method, the CVD method, the droplet-discharge method, or the coating method, and is patterned in the forms of the terminals and the common electrode.

[0052]

Note that, while the resistance configurations Rx and

Ry are formed of the same semiconductor film in the above-described process, the resistance configurations Rx and Ry may be formed of different semiconductor films. In this case, formation and patterning of each semiconductor film is performed separately for each resistance configuration.

[0053]

In the same way, the metal films for the terminals and for the common electrodes may be separately formed for the metal layer.

[0054]

Note that protection circuit configuration as shown in Fig. 4 may be employed as the resistance configuration instead of a resistance layer such as a semiconductor layer, or may be connected to the resistance layer in parallel. Fig. 4 shows an arrangement having a protection circuit configuration employing forward-voltage characteristic and reverse-breakdown-voltage characteristic due to the PN junction of the semiconductor, and a diode-ring configuration wherein ~~a~~ two pairs of diode arrays are connected in parallel, in reverse directions. Each diode can be formed by performing patterning so as to short-circuit the gate and the drain of a MOS transistor, for example, using the MOS process. With the present protection-circuit configuration, in the event that the difference between the voltages applied to both the adjacent

terminals exceeds the withstanding voltage of the diode array, electrostatic current flows from the terminal having higher potential to the terminal having lower potential, thereby releasing static electricity to the adjacent line. The number of the serially-arrayed diodes is determined according to the voltage (e.g., in the range between 10 V and 100 V) which is set to trigger electrostatic protection.

As described above, according to the present first embodiment, with the analog terminals for analog signals and the digital terminals for digital signals, the resistance value of the resistances connected to the analog terminals are relatively increased, and thus, the present first embodiment has the advantage of suppressing cross-talk in the analog terminals to a minimum while maintaining prevention of electrostatic breakdown for all the terminals by providing of the resistances.

[0055]

Furthermore, with the present first embodiment, the resistance value of the resistance between the common electrode and the terminal is relatively reduced as compared with the resistance between the adjacent terminals, and accordingly, electrostatic current to the common electrode is greater than the electrostatic current in the resistance between the adjacent terminals, thereby efficiently protecting the internal circuit of the display panel from

electrostatic discharge.

[0056]

Furthermore, with the present first embodiment, a resistance is provided between an electric power terminal and the adjacent non-electric power terminal, thereby efficiently preventing electrostatic breakdown.

[0057]

Thus, with the circuit substrate of the present first embodiment, the internal circuit of the display panel formed on the glass substrate which tends to be easily charged in the manufacturing step can be protected from electrostatic breakdown. Furthermore, even at the time of use in the final product, the internal circuit within the display panel can be protected against electrostatic discharge which tends to easily occur at each terminal.

[0058]

<Second Embodiment>

A second embodiment according the present invention relates to an EL display panel having the same configuration as with the first embodiment, wherein the layout of the analog terminals and the other terminals is different from the layout in the first embodiment.

[0059]

With the present second embodiment, the scan circuits 12a and 12b are disposed between the cathode line 10a and

the anode line 11a, and between the cathode line 10b and the anode line 11b, respectively, in a plan view shown in Fig. 1. Other components are disposed in the same way as with the first embodiment, and have the same functions as with the first embodiment, so description thereof will be omitted.

[0060]

Fig. 5 is a schematic diagram which illustrates a layout of terminals according to the present second embodiment. In particular, with the present second embodiment, the control signal terminals CX ands CY are disposed between the cathode terminal VC and the anode terminal VR. In order to further simplify description, the great number of identical terminals are not shown in Fig. 5.

[0061]

As shown in Fig. 5, with the present second embodiment, the cathode terminals VC, the control signal terminals CX and CY, the anode terminals VR, VG, and VB, and the data line terminals X1 and X2, are disposed in that order from the outer perimeter to the inner side of the substrate. Of these terminals, the data line terminals serve as analog terminals for transmitting analog signals, and the control signal terminals serve as digital terminals for transmitting digital signals. The cathode terminals are electrically connected to the common electrode, and the anode terminals serve as electric power terminals. Note that in a case that

the electric power of the anode are actively changed, an arrangement may be made wherein the anode terminals serve as digital terminals for a countermeasure against electrostatic breakdown.

[0062]

While the layout of the resistances is generally the same as with the first embodiment (Fig. 2), the difference therewith is that the resistance R2 is disposed between the anode terminal VB and the adjacent data line terminal X1. That is to say, with the present second embodiment, the non-analog terminal adjacent to the digital line terminal X1 which is an analog terminal is the anode terminal VB with low impedance, and accordingly, no digital signals are transmitted in the adjacent non-analog terminal, and accordingly, cross-talk hardly occurs. In this case, there is no problem of cross-talk, so, there is no operational problem due to reduction of the input resistance, and accordingly, there is the advantage in providing a resistance with a small resistance value for prevention of electrostatic breakdown. Accordingly, with the present second embodiment, the resistance between the anode terminal and the data line terminal is set to R2.

[0063]

Other resistance values for the other terminals are set in the same way as with the first embodiment, and

accordingly, description thereof will be omitted. That is to say, the relation of the resistances on the resistance region 120,

$$R1 << R3 < R2 < R4$$

holds, in the same way as with the first embodiment. Note that electrostatic breakdown can be prevented to a certain degree even in the event that the above-described relation is not satisfied.

[0064]

As described above, while the present second embodiment has the same advantages as with the first embodiment, with the present second embodiment, the terminal adjacent to the analog terminal is an electric power terminal which is a non-digital terminal, and accordingly, these adjacent terminals can be connected with a resistance of an even lower resistance value, thereby providing further effects of prevention of electrostatic breakdown.

[0065]

<Third Embodiment>

While a third embodiment of the present invention relates to an EL display panel having the same configuration as with the first embodiment, the layout of the analog terminals and the other terminals is different.

[0066]

With the present third embodiment, a part of the data

lines 13 are disposed between the cathode line 10a and the anode line 11a, and between the cathode line 10b and the anode line 11b, in the plan view shown in Fig. 1. The other configuration is the same as with the first embodiment. The functions of each component are the same as with the first embodiment, so description there of will be omitted.

[0067]

Fig. 6 is a schematic diagram which illustrates a layout of the terminals according to the present third embodiment. In particular, with the present third embodiment, the data line terminals X1 and X2 are disposed between the cathode terminal VC and the anode terminal VR. In order to further simplify description, the great number of identical terminals are not shown in Fig. 6.

[0068]

As shown in Fig. 6, with the present third embodiment, the cathode terminals VC, the data line terminals X1 and X2, the anode terminals VR, VG, and VB, and the control signal terminals CX and CY, are disposed in that order from the outer perimeter to the inner side of the substrate. Of these terminals, the data line terminals serve as analog terminals for transmitting analog signals, and the control signal terminals serve as digital terminals for transmitting digital signals. The cathode terminals are electrically connected to the common electrode, and the anode terminals

serve as electric power terminals. Note that, in a case that the electric power of the anode are actively changed, an arrangement may be made wherein the anode terminals serve as digital terminals for a countermeasure against electrostatic breakdown.

[0069]

While the layout of the resistances is generally the same as with the first embodiment (Fig. 2), the difference therebetween is that the data line terminals X1 and X2 and the ~~anode~~ cathode terminals VC and anode terminals VR are disposed adjacent one to another, respectively. That is to say, with the present third embodiment, the non-analog terminal adjacent to the data line terminal X1 which is an analog terminal is the cathode terminal VC with low impedance, and the non-analog terminal adjacent to the data line terminal X2 which is an analog terminal is the anode terminal VR which is an electric power terminal with low impedance. No digital signals are transmitted in either of the electrode terminals, and accordingly, hardly any cross-talk occurs between both electrode lines and the data line. There is no problem of cross-talk, so there are no operational problems due to reduction of the input resistance, and accordingly, there is the advantage in providing a resistance with a small resistance value for prevention of electrostatic breakdown. Accordingly, with

the present third embodiment, the resistance between: each of the cathode terminal and the anode terminal; and the adjacent data ~~line~~terminal; is set to R2.

[0070]

Other resistance values for the other terminals are set in the same way as with the first embodiment, and accordingly, description thereof will be omitted. That is to say, the relation of the resistance values on the resistance region 120,

$R1 << R3 < R2 < R4$

holds, in the same way as with the first embodiment. Note that electrostatic breakdown can be prevented to a certain degree even in the event that the above-described relation is not satisfied.

[0071]

As described above, while the present third embodiment has the same advantages as with the first embodiment, with the present third embodiment, the terminal adjacent to the analog terminal is an electric power terminal which is a non-digital terminal, and accordingly, the adjacent terminal can be connected with a resistance of an even lower resistance value, thereby providing further effects of prevention of electrostatic breakdown.

[0072]

In particular, the data lines for transmitting analog

signals, disposed adjacent to non-analog lines for transmitting digital signals, tend to be easily influenced, leading to cross-talk. However, with the present embodiment, the data lines are disposed so as to be introduced between the electric power lines, and so as to be distanced from the control signal terminals for transmitting digital signals, thereby efficiently maintaining prevention of electrostatic breakdown.

[0073]

<Fourth Embodiment>

A fourth embodiment of the present invention relates to an EL display panel which is an electro-optical device employing a circuit substrate described in the above embodiments.

[0074]

Fig. 7 illustrates a substantive circuit diagram of the display panel 1 according to the present embodiment. The display panel of the present fourth embodiment comprises a light-emission layer OLED, which can emit light for each pixel region due to the electro-luminescence effect, holding capacitance C for driving the light-emission layer OLED, and thin-film-transistors T1 and T2. The scan circuit 12 provides scan lines Vsel(14) to each of the pixel regions. Furthermore, an unshown external D/A converter supplies analog signals to data lines Vsig(13) through the terminals.

The anodes line corresponds to Vdd. The current for each pixel region is controlled by controlling the scan lines Vsel and the data lines Vsig, thereby controlling light emission from the light-emission layer OLED.

[0075]

Note that the aforementioned driving circuit is an example of circuits employing EL deices for light-emission components, and other circuit configurations may be employed. Furthermore, an arrangement may be made wherein a liquid crystal display device is employed for a light-emission component by suitably modifying the circuit configuration.

[0076]

In particular, the present fourth embodiment has a configuration wherein the resistance region 102 is formed on the area where the terminals corresponding to the input terminals for each of signals and electric power have been formed, thereby providing electrostatic protection as described in the first embodiment through the third embodiment. That is to say, with the display panel according to the present embodiment, the inner circuits such as pixel circuits and the ~~driving~~ scanning circuits can be efficiently protected from electrostatic breakdown during manufacturing or at the time of use in the final product due to the functions of the substrate circuit of the present invention.

[0077]

<Fifth Embodiment>

A present fifth embodiment relates to an electronic apparatus employing a display panel which comprises the electro-optical device as described in the above embodiment 4.

The electro-optical device employing the circuit substrate according to the present invention can be applied to various types of electronic apparatuses. Figs. 8(a) through 8(f) illustrate examples of electronic apparatuses to which the display panel 1 according to the present invention can be applied.

[0078]

Fig. 8(a) shows an example wherein the present invention is applied to a cellular phone, wherein the cellular phone 30 comprises an antenna unit 31, an audio output unit 32, an audio input unit 33, an operating unit 34, and the display panel 1 according to the present invention. As described above, the display panel according to the present invention can be applied to a display unit of a cellular phone.

[0079]

Fig. 8(b) shows an example wherein the present invention is applied to a video camera, wherein the video camera 40 comprises a TV camera unit 41, an operating unit

42, an audio input unit 43, and the display panel 1 according to the present invention. As described above, the display panel according to the present invention can be applied to a viewfinder or a display unit of a video camera.

[0080]

Fig. 8(c) shows an example wherein the present invention is applied to a portable personal computer, wherein the portable personal computer 50 comprises a camera unit 51, an operating unit 52, and the display panel 1 according to the present invention. As described above, the display panel according to the present invention can be applied to a display unit of a computer.

[0081]

Fig. 8(d) shows an example wherein the present invention is applied to a head mount display, wherein the head mount display 60 comprises a belt 61, an optical system storage unit 62, and the display panel 1 according to the present invention. As described above, the display panel according to the present invention can be applied to an image display unit of a head mount display.

[0082]

Fig. 8(e) shows an example wherein the present invention is applied to a rear projector, wherein the rear projector 70 comprises casing 71, a light source 72, synthesizing optical system 73, a mirrors 74 and 75, a

screen 76, and the display panel 1 according to the present invention. As described above, the display panel according to the present invention can be applied to an image display unit of a rear projector.

[0083]

Fig. 8(f) shows an example wherein the present invention is applied to a front projector, wherein the projector 80 comprises casing 82, an optical system 81, and the display panel 1 according to the present invention, wherein an image can be displayed on a screen 83. As described above, the display panel according to the present invention can be applied to an image display unit of a front projector.

[0084]

Arrangements employing the present invention are not restricted to the above-described examples, but rather, the present invention can be applied to various types of electronic apparatuses. Examples to which the present invention can be applied, other than the above-described examples, include facsimile apparatuses with display functions, digital camera viewfinders, portable TV sets, DSP devices, PDAs, palmtops, electronic signboards, and advertising displays.

[0085]

[Advantages]

With the present invention, resistances connected to analog terminals have resistance values greater than those between digital terminals, thereby providing the advantage of suppressing cross-talk to a minimum in the analog terminals while maintaining prevention of electrostatic breakdown due to the resistance in all terminals.

[0086]

Furthermore, with an arrangement according to the present invention, wherein a first resistance and a second resistance are connected to the terminal in parallel, even in the event that the first resistance between the analog terminal and the adjacent terminal have a somewhat great resistance value, the total resistance value formed of the resistances connected in parallel is greatly reduced, thereby providing efficient prevention of electrostatic breakdown.

[0087]

Thus, with the present invention, the internal circuit of the circuit substrate can be efficiently protected from electrostatic discharge occurring due to electrostatic charging of the substrate during manufacturing. Furthermore, even at the time of use in the final product, the internal circuit can be efficiently protected from electrostatic discharge which tends to occur at each terminal.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a plan view which illustrates a circuit layout of a circuit substrate according to a first embodiment of the present invention.

[Fig. 2]

Fig. 2 is a schematic diagram which illustrates a circuit layout on a resistance region according to the first embodiment.

[Fig. 3]

Figs. 3(a) through 3(e) illustrate an example of a resistance configuration according to the first embodiment, wherein Fig. 3(a) is a fragmentary enlarged plan view thereof, and Figs. 3(b) through 3(e) are cross-sectional views taken along lines B-B, C-C, D-D, and E-E, respectively, in Fig. 3(a).

[Fig. 4]

Fig. 4 shows an example of a protection circuit formed of diode arrays, which is a modification of the resistance according to the present invention.

[Fig. 5]

Fig. 5 is a schematic diagram which illustrates a circuit layout on a resistance region according to a second embodiment.

[Fig. 6]

Fig. 6 is a schematic diagram which illustrates a

circuit layout on a resistance region according to a third embodiment.

[Fig. 7]

Fig. 7 is a schematic diagram which illustrates a circuit layout of a display panel which is an electro-optical device according to a fourth embodiment.

[Fig. 8]

Figs. 8(a) through 8(f) show examples of electronic apparatuses according to the fifth embodiment showing examples in which the display panel of the present invention is applied, wherein Fig. 8(a) illustrates a cellular phone, Fig. 8(b) illustrates a video camera, Fig. 8(c) illustrates a portable personal computer, Fig. 8(d) illustrates a head mount display, Fig. 8(e) illustrates a rear projector, and Fig. 8(f) illustrates a front projector.

[Reference Numerals]

R1 through R5: resistance (protection circuit)

T1 through T9: terminal

VC: cathode terminal

VR, VG, VB: anode terminal

CX, CY: control signal terminal

X1, X2: data line terminal

1: circuit substrate

10: cathode line

11: anode line

12: scan circuit

13: data line

14: scan line

15: metal layer

101: common electrode

102: resistance region

[Name of Document] ABSTRACT

[Abstract]

[Object] To provide a circuit substrate including an electrostatic-breakdown-protection circuit efficient for an EL display panel or the like.

[Solving Means] A substrate (100) comprises a common electrode (101) formed on the perimeter of the substrate (100), multiple terminals (T) formed on the substrate (100), one or more first resistances (R3, R4) formed between adjacent terminals, and one or more second resistances (R1, R2) formed between the terminals (T) and the common electrode (101). The terminal (T) is connected to both the first resistance and the second resistance, wherein the first resistance has a resistance value greater than the second resistance.

[Selected Figure] Fig. 2

FIG. 1

12a, 12b SCANNING CIRCUIT

FIG. 2

CATHODE ANODE CONTROL SIGNALS DATA LINES

FIG. 5

CATHODE CONTROL SIGNALS ANODE DATA LINES

FIG. 6

CATHODE DATA LINES ANODE CONTROL SIGNALS

FIG. 7

12 SCANNING CIRCUIT

TERMINAL GROUP

Fig. 1

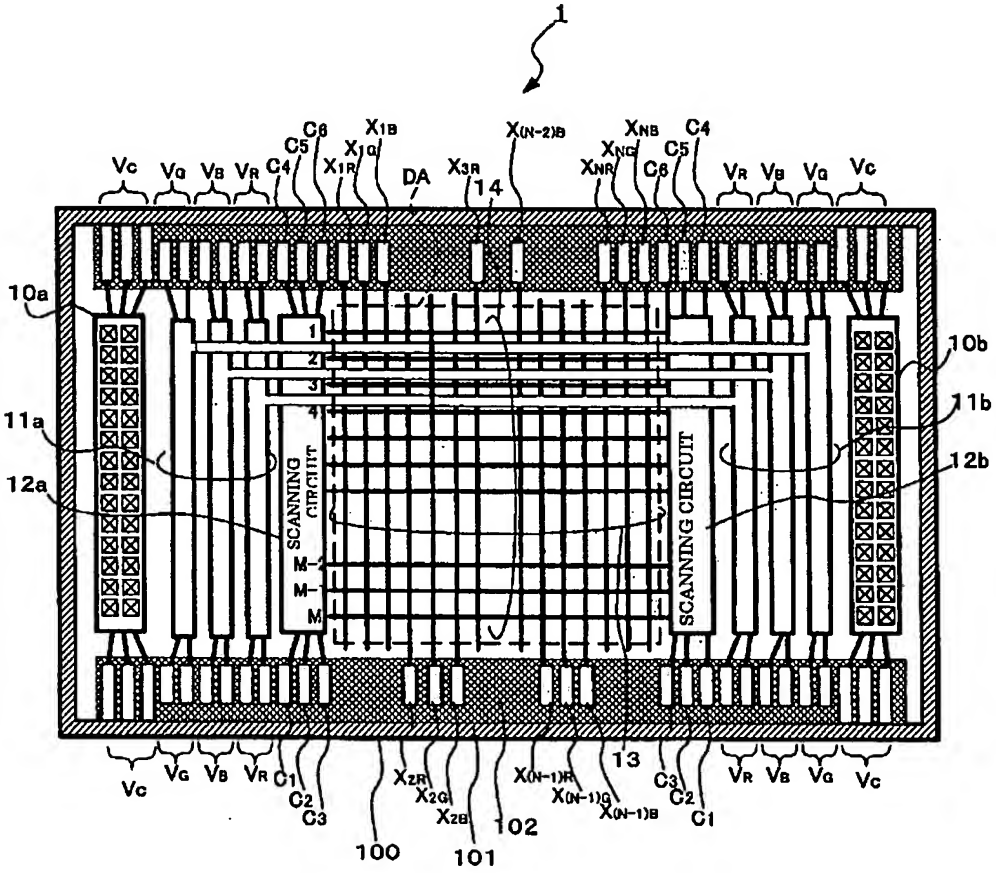


Fig. 2

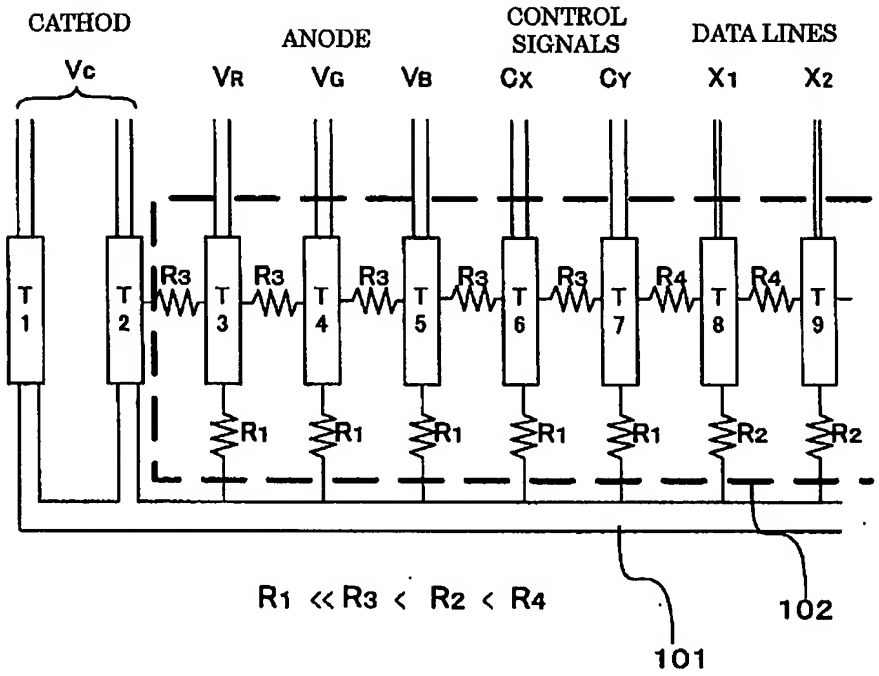
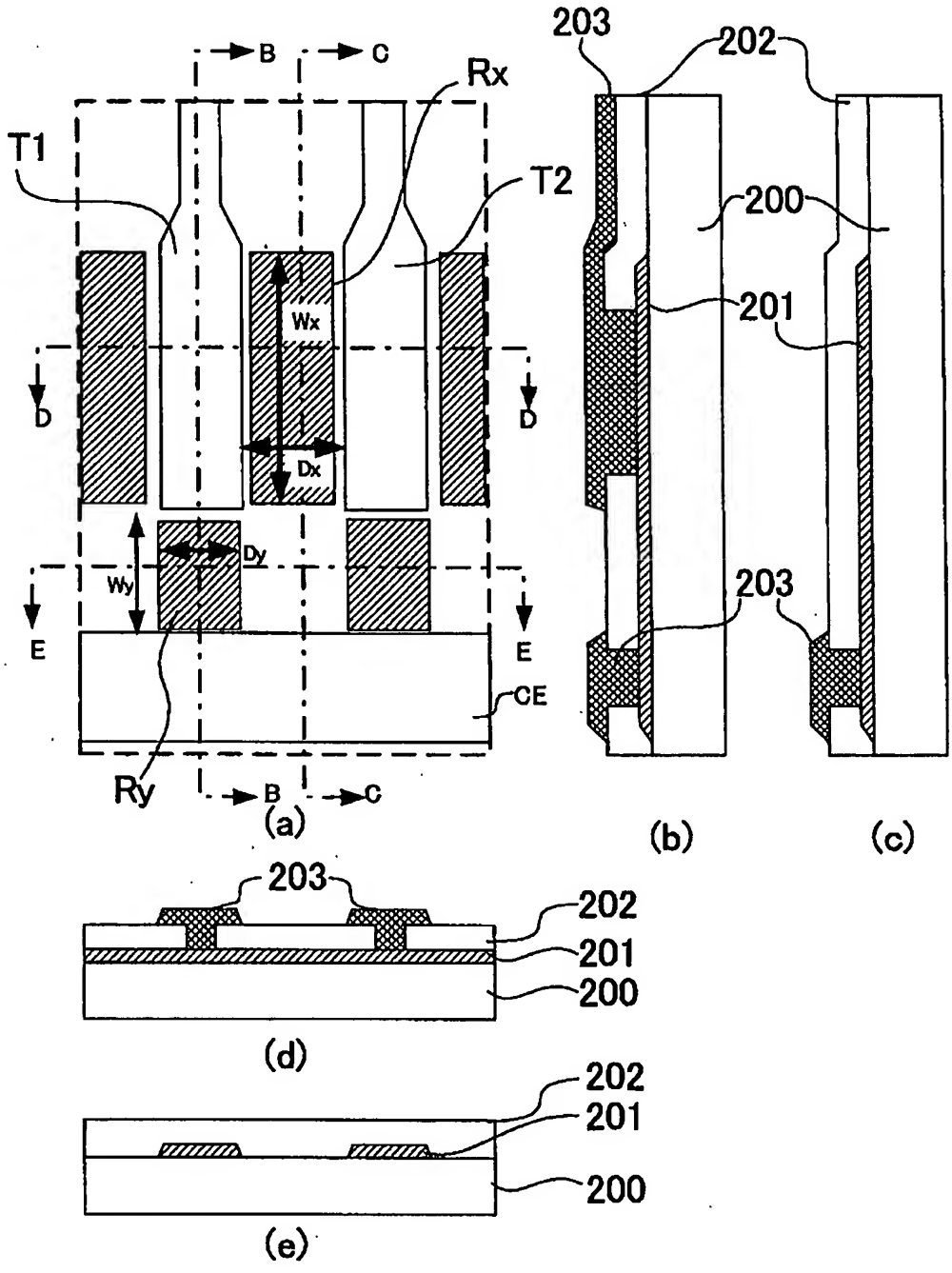

CATHOD
Vc
ANODE
VR
VG
VB
CONTROL SIGNALS
CX
CY
DATA LINES
X1
X2
T1
T2
T3
T4
T5
T6
T7
T8
T9
R3
R4
R1
R2
R1 << R3 < R2 < R4
101
102

Fig. 3


B
C
Rx
T1
T2
Wx
D
D
Dx
Dy
Wy
E
E
CE
Ry
B
C
(a)
203
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(b)
(c)
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201
200
(d)
202
201
200
(e)

Fig. 4

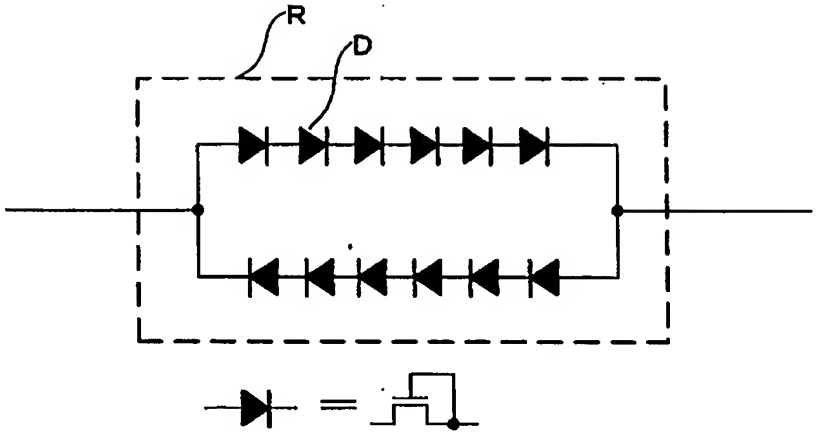
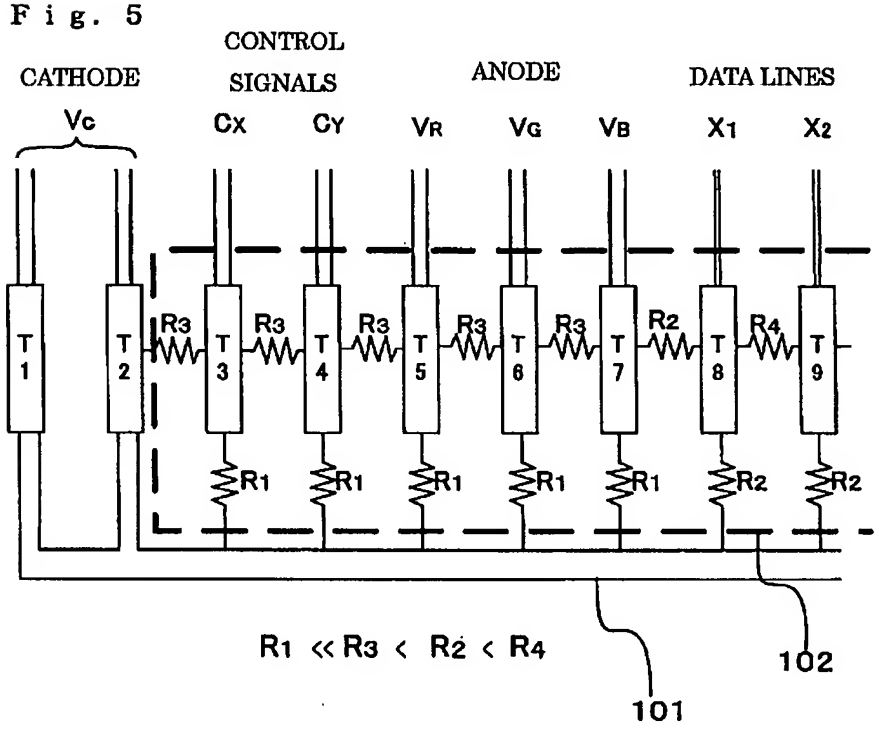

R
D

Fig. 5


CONTROL SIGNALS
CATHODE
ANODE
DATA LINES
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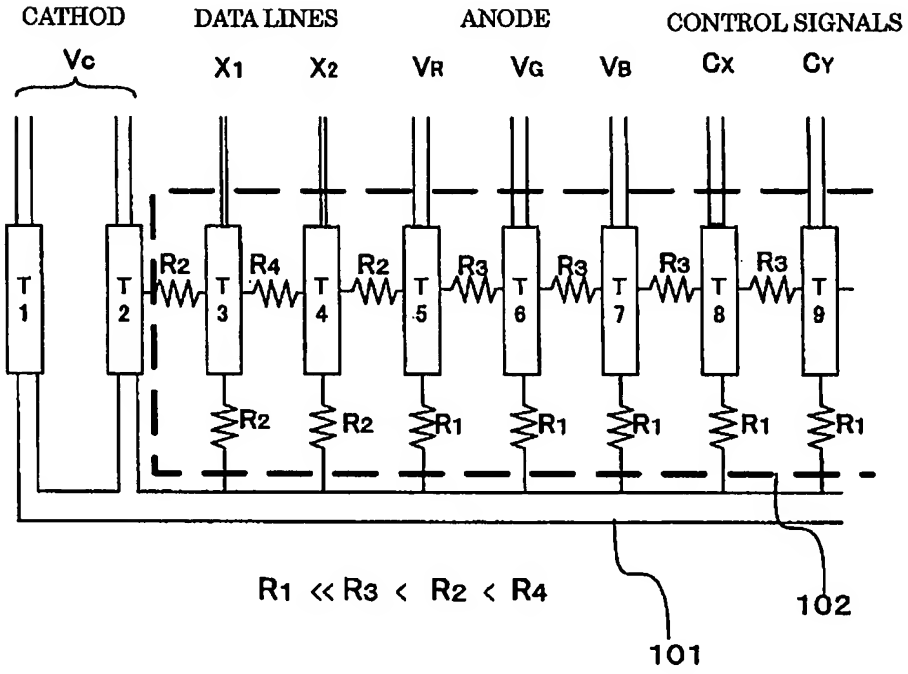
Cx
Cy
VR
VG
VB
X1
X2
T1
T2
T3
T4
T5
T6
T7
T8
T9
R3
R2
R4
R1
R1 ≪ R3 < R2 < R4
101
102

Fig. 6


CATHOD
Vc
DATA LINES
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X2
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VR
VG
VB
CONTROL SIGNALS
CX
CY
T1
T2
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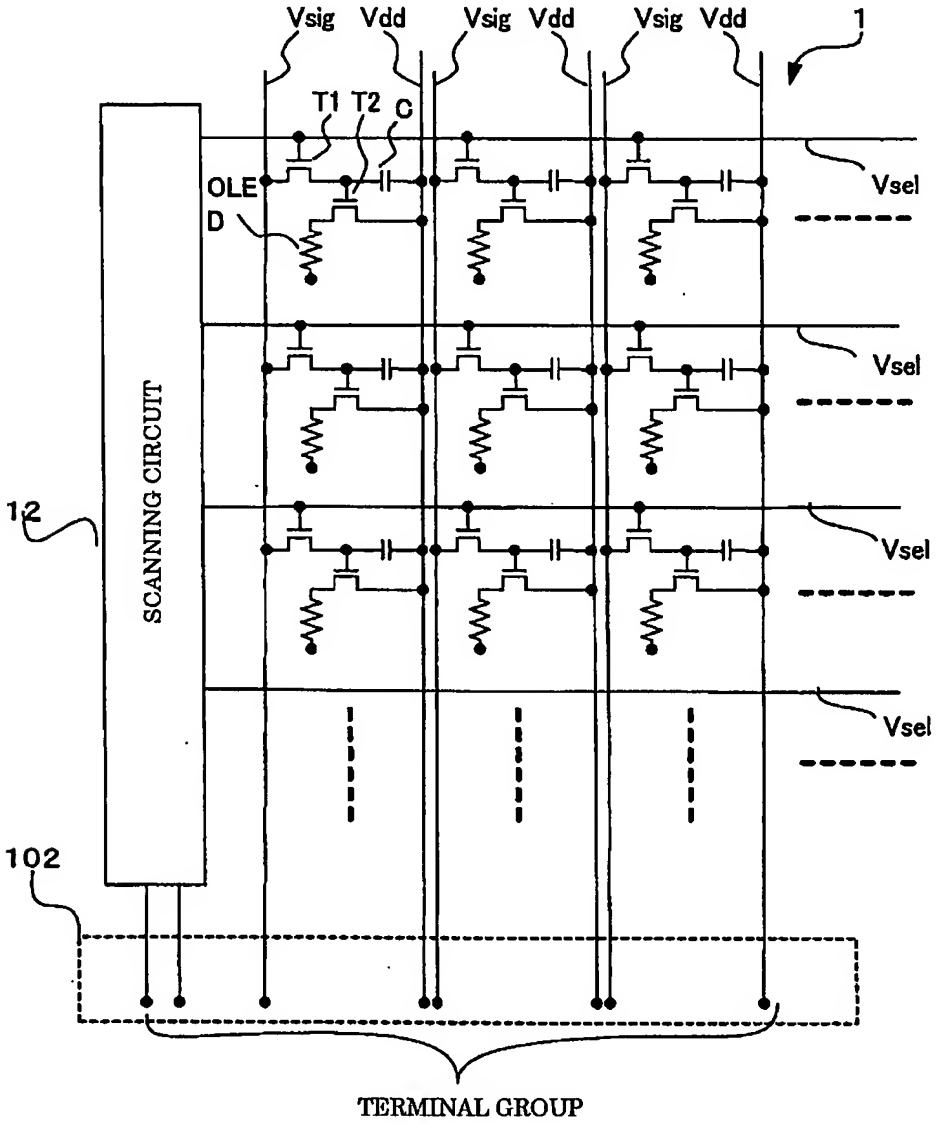
T4
T5
T6
T7
T8
T9
R2
R4
R2
R3
R3
R3
R3
R2
R2
R1
R1
R1
R1
R1
R1 << R3 < R2 < R4
101
102

Fig. 7


Vsig
Vdd
Vsig
Vdd
Vsig
Vdd
1
T1
T2
C
OLE
D
Vsel
Vsel
Vsel
Vsel
SCANNING CIRCUIT
12
102
TERMINAL GROUP

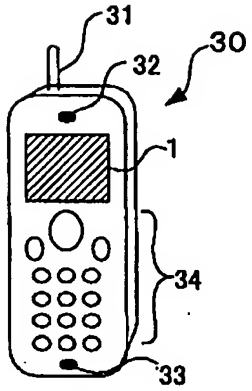


Fig. 8A

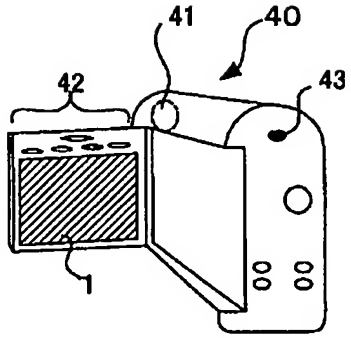


Fig. 8B

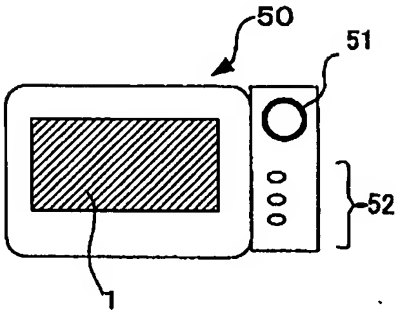


Fig. 8C

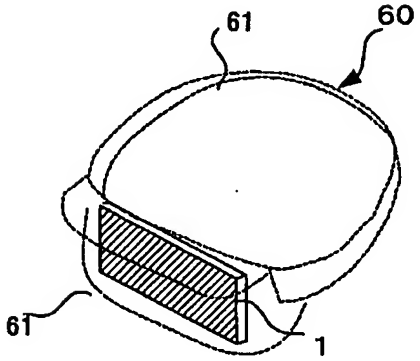


Fig. 8D

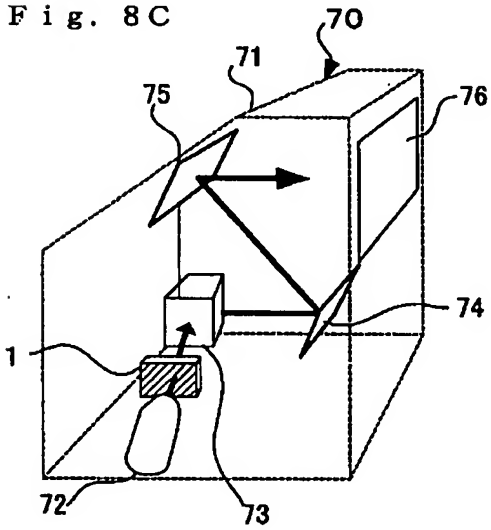


Fig. 8E

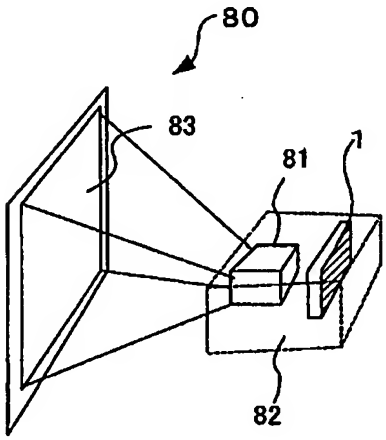


Fig. 8F